

INFORMATION DISCLOSURE CITATION

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ATTY DOCKET NO.

FIS920030245

SERIAL NO.

10/708,430

FILING DATE

3/3/04

GROUP

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
ah	6,228,694	5/8/01	Doyle et al.			
	6,406,973	6/18/02	Lee			
	6,281,532	8/28/01	Doyle et al.			
	5,683,934	11/4/97	Candelaria			
	6,368,931	4/9/02	Kuhn et al.			
	5,310,446	5/10/94	Konishi et al.			
	4,853,076	8/1/89	Tsaur et al.			
	2002/0090791	7/11/02	Doyle et al.			
	2002/0074598	6/20/02	Doyle et al.			
	6,509,618	1/21/03	Jan et al.			
ah	6,476,462	11/5/02	Shimizu et al.			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
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Alh	6,362,082	3/26/02	Doyle et al.			
	6,228,694	5/8/01	Doyle et al.			
	5,565,697	10/15/96	Asakawa et al.			
	2003/0040158	2/27/03	Saitoh			
	2002/0086472	7/4/02	Roberds et al.			
	6,521,964	2/18/03	Jan et al.			
	6,506,652	1/14/03	Jan et al.			
	5,081,513	1/14/92	Jackson et al.			
	3,602,841	8/31/71	McGroddy			
	6,531,740	3/11/03	Bosco et al.			
Alh	6,531,369	3/11/03	Ozkan et al.			

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Anders Kuyper

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Alh	6,501,121	12/31/02	Yu et al.			
	6,498,358	12/24/02	Lach et al.			
	6,493,497	12/10/02	Ramdani et al.			
	6,403,975	6/11/02	Brunner et al.			
	6,361,885	3/26/02	Chou			
	6,255,169	7/3/01	Li et al.			
	6,246,095	6/12/01	Brady et al.			
	6,165,383	12/26/00	Chou			
	6,133,071	10/17/00	Nagai			
	6,046,464	4/4/00	Schetzina			
Alh	6,025,280	2/15/00	Brady et al.			

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Andr. Kucera

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Alh	5,940,736	8/17/99	Brady et al.			
	5,880,040	3/9/99	Sun et al.			
	5,861,651	1/19/99	Brasen et al.			
	5,679,965	10/21/97	Schetzina			
	5,670,798	9/23/97	Schetzina			
	5,561,302	10/1/96	Candelaria			
	5,471,948	12/5/95	Burroughes et al.			
	5,459,346	10/17/95	Asakawa et al.			
	5,391,510	2/21/95	Hsu et al.			
	5,371,399	12/6/94	Burroughes et al.			
Alh	5,108,843	4/28/92	Ohtaka et al.			

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Alh	5,060,030	10/22/91	Hoke			
	4,958,213	9/18/90	Eklund et al.			
	4,665,415	5/12/87	Esaki et al.			
	5,989,978	11/23/99	Peidous			
	6,284,626	9/4/01	Kim			
	6,274,444	8/14/01	Wang			
	6,261,964	7/17/01	Wu et al.			
	6,221,735	4/24/01	Manley el al.			
	6,117,722	9/12/00	Wuu et al.			
	6,107,143	8/22/00	Park et al.			
Alh	6,090,684	7/18/00	Ishitsuka et al.			

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*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
ah	6,066,545	5/23/00	Doshi et al.			
	6,008,126	12/28/99	Leedy			
	5,946,559	8/31/99	Leedy			
	5,840,593	11/24/98	Leedy			
	5,592,018	1/7/97	Leedy			
	5,592,007	1/7/97	Leedy			
	5,571,741	11/5/96	Leedy			
	5,557,122	9/17/96	Shirvastava et al.			
	5,354,695	10/11/94	Leedy			
	5,134,085	7/28/92	Gilgen et al.			
aa	5,006,913	4/9/91	Sugahara et al.			

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Andy Murray

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Alh	4,952,524	8/28/90	Lee et al.			
	4,855,245	8/8/89	Neppl et al.			
	2002/0086497	7/4/02	Kwok			
	5,960,297	9/28/99	Saki			
	6,403,486	6/11/02	Lou			
	6,284,623	9/4/01	Zhang et al.			
	2003/0032261	2/13/03	Yeh et al.			
	2003/0057184	3/27/03	Yu et al.			
	6,265,317	7/24/01	Chiu et al.			
	2003/0067035	4/10/03	Tews et al.			
Alh	6,461,936	10/8/02	von Ehrenwall			

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Al	6,319,794	11/20/01	Akatsu et al.			
Al	20010009784	7/26/01	Ma et al.			

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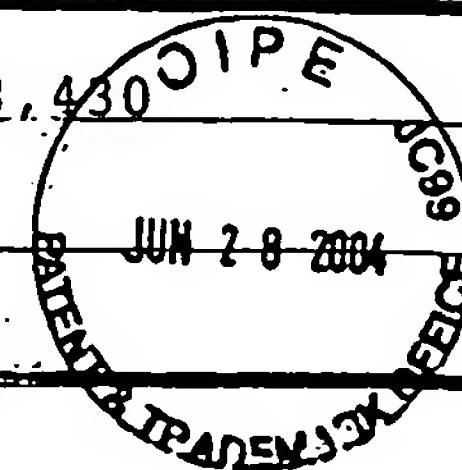
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S
INFORMATION DISCLOSURE STATEMENTApplicant:
Michael P. Belyansky, et al.

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ah		Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si n-MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
		Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
		Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
		F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
		Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
		A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
ah		K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

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